WHAT IS CLAIMED IS:

1. A communication apparatus, comprising:

a transmitter including an encoder circuit for converting transmit data into a transmit signal synchronizing to a transmit clock;

a receiver including a decoder circuit for converting a receive signal into receive data synchronizing to a receive clock; and

a clock supply select circuit controlling a supply of said transmit clock and said receive clock to said transmitter and said receiver,

said clock supply select circuit including

a clock generate circuit generating an internal clock signal, and

a clock modulate circuit generating a modulate clock signal that is modulated such that at least one of frequency error, phase fluctuation, jitter and waveform fluctuation is forcibly applied to said internal clock of reference, wherein

in a normal operation mode, said clock supply select circuit supplies said internal clock signal as each of said transmit clock and said receive clock in common, and in a loopback operation mode, said clock supply select circuit supplies said internal clock signal as one of said transmit clock and said receive clock and supplies said modulate clock signal as the other of said transmit clock and said receive clock.

2. The communication apparatus according to claim 1, wherein

said clock supply select circuit includes a clock switch provided corresponding to said transmitter, wherein

said clock switch supplies to said transmitter, in said normal operation mode, said internal clock signal as said transmit clock, and in said loopback operation mode, said modulate clock signal as said transmit clock, and wherein

said clock supply select circuit supplies to said receiver, in each of said normal operation mode and said loopback operation mode, said internal clock signal as said receive clock.

3. The communication apparatus according to claim 1, wherein

said clock supply select circuit includes a clock switch provided corresponding to said receiver, wherein

said clock switch supplies to said receiver, in said normal operation mode, said internal clock signal as said receive clock, and in said loopback operation mode, said modulate clock signal as said receive clock, and wherein

said clock supply select circuit supplies to said transmitter, in each of said normal operation mode and said loopback operation mode, said internal clock signal as said transmit clock.

4. The communication apparatus according to claim 1, wherein

said clock generate circuit further generates a plurality of clock signals having a same frequency as said internal clock signal and with phases different from each other, and wherein

said clock modulate circuit includes

a counter circuit of which count value changes synchronizing to an external trigger, and

a selector circuit receiving said plurality of clock signals from said clock generate circuit and selectively outputting one of said plurality of clock signals that corresponds to said count value as said modulate clock signal.

5. The communication apparatus according to claim 1, further comprising

a data compare circuit comparing said transmit data input to said encoder circuit and said receive data output from said decoder circuit, and generating a signal in accordance with a result of the comparison.

6. The communication apparatus according to claim 5, wherein

said data compare circuit includes

a buffer circuit receiving said transmit data, retaining said transmit data inside for a period in accordance with a timing difference between said internal clock signal and said modulate clock signal, and outputting said

transmit data, and

a comparator comparing said transmit data output from said buffer circuit and said receive data from said decoder circuit.

7. The communication apparatus according to claim 1, wherein

said transmitter further includes a differential driver converting said transmit signal of a single-end signal into a differential signal to be output, and wherein

said receiver further includes a differential receiver converting a received differential signal into said receive signal of a single-end signal;

said communication apparatus further comprising

a signal switch forming as necessary, in said loopback operation mode, a signal path bypassing said differential driver and said differential receiver for passing said transmit signal output from said encoder circuit directly as said receive signal.

8. A communication apparatus, comprising:

a transmitter including an encoder circuit converting transmit data into a transmit signal synchronizing to said clock signal;

a receiver including a decoder circuit converting a receive signal into receive data synchronizing to said clock signal;

a clock generate circuit generating a plurality of clock signals having a same frequency as said clock signal and with phases different from each other; and

a jitter measure circuit measuring, in a loopback operation mode, jitter occurring in said transmitter, based on a transition of a result of phase comparison between a transition edge of said receive signal and a transition edge of each of said plurality of clock signals.

9. The communication apparatus according to claim 8, wherein

said jitter measure circuit includes

a clock sampling circuit detecting each level of said plurality of clocks at each of said transition edges of said receive signal, and

a phase compare circuit converting a transition of the level of said plurality of clocks between each of said transition edges of said receive signal, detected by said clock sampling circuit, into a phase difference.

10. The communication apparatus according to claim 9, wherein said phase compare circuit generates a detect signal indicating whether said phase difference obtained by converting the transition of the level of said plurality of clocks exceeds a prescribed jitter tolerance value.

11. The communication apparatus according to claim 8, wherein said transmitter further includes a differential driver converting said transmit signal of a single-end signal into a differential signal to be output, and wherein

said receiver further includes a differential receiver converting a received differential signal into said receive signal of a single-end signal;

said communication apparatus further comprising

a signal switch forming as necessary, in said loopback operation mode, a signal path bypassing said differential driver and said differential receiver for passing said transmit signal output from said encoder circuit directly as said receive signal.

12. A communication apparatus, comprising:

a communication node and a test communication node capable of transmitting and receiving a signal between other said communication apparatus;

a transmitter converting received transmit data into a transmit signal and outputting it to said communication node;

a receiver converting a receive signal that is received at a receive node and outputting the converted receive signal as receive data; and

a signal switch selectively forming a signal path between one of said communication node and said test communication node, and said receive node; wherein

in a first test mode, a signal path is formed between said

communication node of said communication apparatus and said test communication node of said other communication apparatus, as well as between said test communication node of said communication apparatus and said communication node of said other communication apparatus, and wherein

within each of said communication apparatus and said other communication apparatus, said signal switch forms a signal path between said test communication node and said receive node.

13. The communication apparatus according to claim 12, wherein

in each of a second test mode that is different from said first test mode and a normal operation mode, said signal switch of said communication apparatus forms a signal path between said communication node and said receive node of said communication apparatus.

14. The communication apparatus according to claim 12, wherein

said transmitter and said receiver operates synchronizing to a transmit clock and a receive clock, respectively;

said communication apparatus further comprising

a clock supply select circuit controlling a supply of said transmit clock and said receive clock to said transmitter and said receiver; wherein

said clock supply select circuit includes

a clock generate circuit generating an internal clock signal, and

a clock modulate circuit generating a modulate clock signal that is modulated such that at least one of frequency error, phase fluctuation, jitter and waveform fluctuation is applied to said internal clock signal of reference, and wherein

in said normal operation mode, said clock supply select circuit supplying said internal clock signal as each of said transmit clock and said receive clock in common, and in said first test mode, said clock supply select circuit supplying said internal clock signal as one of said transmit clock and said receive clock, and said modulate clock signal as the other of said transmit clock and said receive clock.

15. The communication apparatus according to claim 12, wherein

said transmitter includes an encoder circuit converting said transmit data into said transmit signal synchronizing to a clock signal, and wherein

said receiver includes a decoder circuit converting said receive signal into said receive data synchronizing to said clock signal;

said communication apparatus further comprising

a clock generate circuit generating a plurality of clock signals having a same frequency as said clock signal and with phases different from each other, and

a jitter measure circuit measuring, in said first test mode, jitter occurring in said transmitter based on a transition of a result of phase comparison between a transition edge of said receive signal and a transition edge of said plurality of clock signals.